ABSTRACT

A self-configuring processing element for providing arbitrarily wide, application-specific instruction set extensions to an Instruction Set Architecture (ISA) microcontroller includes a System Bus Interface and Instruction Handler (SBI), an Input Router and Conditioner (IRC), an ALU, a Memory, and an Output Router. The SBI may accept address, data and control signals and may include a unique address decoder, an instruction register that decodes address and data bits, a state machine for sequencing through initialization and instruction set-up, and transceivers for controlling data flow with the system bus and feedback. The IRC may select information to transmit to the ALU and/or the Memory and may include circuitry for registering, shifting, incrementing, and decrementing inputted information. The ALU and the Memory may perform operations on the output of the IRC. The Output Router may route the output of the ALU and/or the Memory to one or more possible destinations.